

FCB20N60F

N-Channel SuperFET® FRFET® MOSFET

600 V, 20 A, 190 mΩ

Features

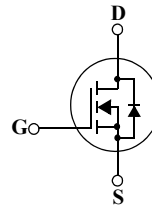
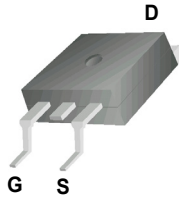
- 650V @T_J = 150°C
- Typ. R_{DS(on)} = 150 mΩ
- Ultra Low Gate Charge (Typ. Q_g = 75 nC)
- Low Effective Output Capacitance (Typ. C_{oss,eff} = 165 pF)
- 100% Avalanche Tested
- RoHS Compliant

Application

- Lighting
- Solar Inverter
- AC-DC Power Supply

Description

SuperFET® MOSFET is Fairchild Semiconductor®'s first generation of high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently, SuperFET MOSFET is very suitable for the switching power applications such as PFC, server/telecom power, FPD TV power, ATX power and industrial power applications. SuperFET FRFET® MOSFET's optimized body diode reverse recovery performance can remove additional component and improve system reliability.



MOSFET Maximum Ratings T_C = 25°C unless otherwise noted*

Symbol	Parameter	FCB20N60F	Unit
V _{DSS}	Drain to Source Voltage	600	V
I _D	Drain Current	-Continuous (T _C = 25°C)	20
		-Continuous (T _C = 100°C)	12.5
I _{DM}	Drain Current	- Pulsed (Note 1)	60
V _{GSS}	Gate to Source Voltage	±30	V
E _{AS}	Single Pulsed Avalanche Energy	(Note 2)	690
I _{AR}	Avalanche Current	(Note 1)	20
E _{AR}	Repetitive Avalanche Energy	(Note 1)	20.8
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	50
P _D	Power Dissipation	(T _C = 25°C)	208
		- Derate above 25°C	1.67
T _J , T _{STG}	Operating and Storage Temperature Range	-55 to +150	°C
T _L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300	°C

Thermal Characteristics

Symbol	Parameter	FCB20N60F	Unit
R _{θJC}	Thermal Resistance, Junction to Case, Max	0.6	°C/W
R _{θJA} *	Thermal Resistance, Junction to Ambient, Max*	40	
R _{θJA}	Thermal Resistance, Junction to Ambient, Max	62.5	

* When mounted on the minimum pad size recommended (PCB Mount)

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FCB20N60F	FCB20N60FTM	D ² -PAK	330mm	24m	800

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}, T_C = 25^\circ\text{C}$	600	-	-	V
		$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}, T_C = 150^\circ\text{C}$	-	650	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C	-	0.6	-	V/ $^\circ\text{C}$
BV_{DS}	Drain-Source Avalanche Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 20\text{ A}$	-	700	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$	-	-	1	μA
		$V_{DS} = 480\text{ V}, V_{GS} = 0\text{ V}, T_C = 125^\circ\text{C}$	-	-	10	
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 30\text{ V}, V_{DS} = 0\text{ V}$	-	-	± 100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	3.0	-	5.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 10\text{ A}$	-	0.15	0.19	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 40\text{ V}, I_D = 10\text{ A}$ (Note 4)	-	17	-	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}$ $f = 1.0\text{ MHz}$	-	2370	3080	pF
C_{oss}	Output Capacitance		-	1280	1665	pF
C_{rfs}	Reverse Transfer Capacitance		-	95	-	pF
C_{oss}	Output Capacitance	$V_{DS} = 480\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	-	65	85	pF
$C_{oss\text{eff}}$	Effective Output Capacitance	$V_{DS} = 0\text{ V to } 400\text{ V}, V_{GS} = 0\text{ V}$	-	165	-	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 300\text{ V}, I_D = 20\text{ A}$ $R_G = 25\ \Omega$	-	62	135	ns	
t_r	Turn-On Rise Time		-	140	290	ns	
$t_{d(off)}$	Turn-Off Delay Time		-	230	470	ns	
t_f	Turn-Off Fall Time		(Note 4, 5)	-	65	140	ns
$Q_{g(tot)}$	Total Gate Charge at 10V		$V_{DS} = 480\text{ V}, I_D = 20\text{ A},$ $V_{GS} = 10\text{ V}$	-	75	98	nC
Q_{gs}	Gate to Source Gate Charge	(Note 4, 5)	-	13.5	18	nC	
Q_{gd}	Gate to Drain "Miller" Charge		-	36	-	nC	

Drain-Source Diode Characteristics

I_S	Maximum Continuous Drain to Source Diode Forward Current	-	-	20	A	
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	60	A	
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_{SD} = 20\text{ A}$	-	-	1.4	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_{SD} = 20\text{ A}$ $di_F/dt = 100\text{ A}/\mu\text{s}$ (Note 4)	-	160	-	ns
Q_{rr}	Reverse Recovery Charge		-	1.1	-	μC

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. $I_{AS} = 10\text{ A}, V_{DD} = 50\text{ V}, R_G = 25\ \Omega$, Starting $T_J = 25^\circ\text{C}$
3. $I_{SD} \leq 20\text{ A}, di/dt \leq 1200\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
4. Pulse Test: Pulse width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$
5. Essentially Independent of Operating Temperature Typical Characteristics

Typical Performance Characteristics

Figure 1. On-Region Characteristics

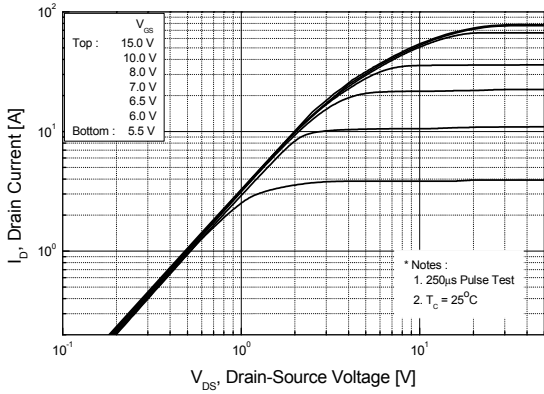


Figure 2. Transfer Characteristics

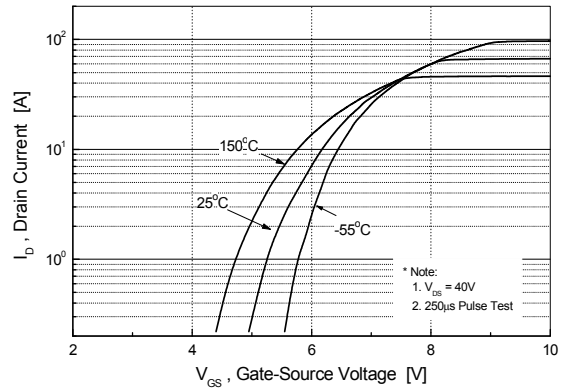


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

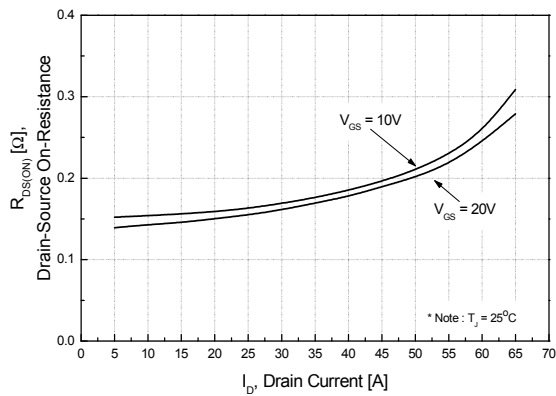


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

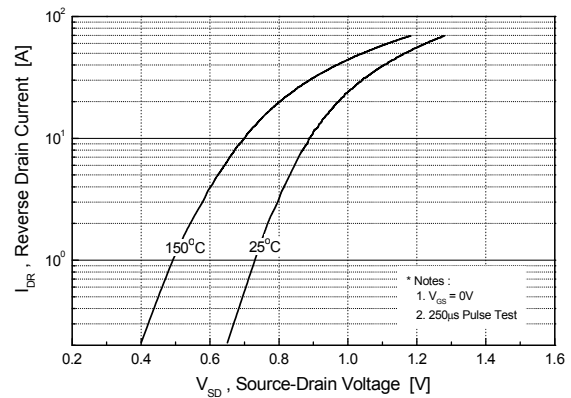


Figure 5. Capacitance Characteristics

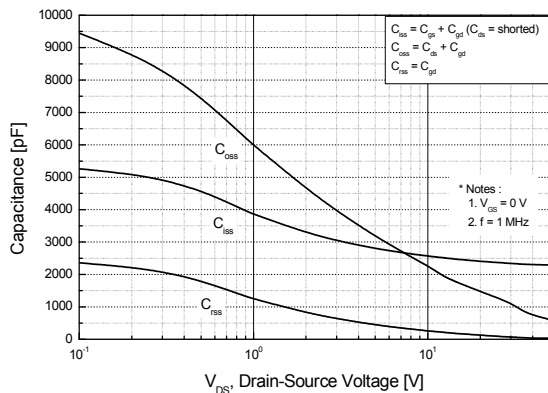
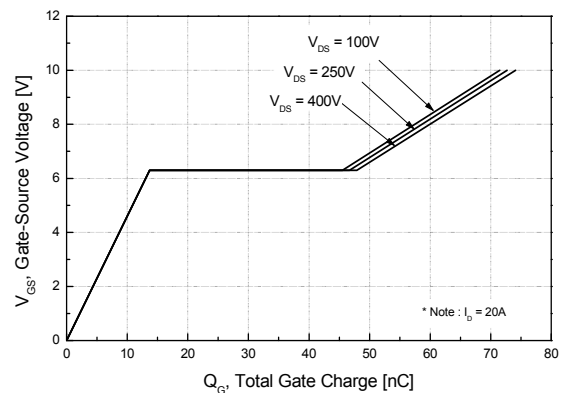


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

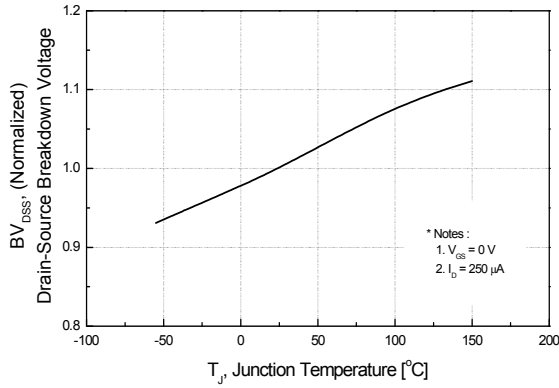


Figure 8. On-Resistance Variation vs. Temperature

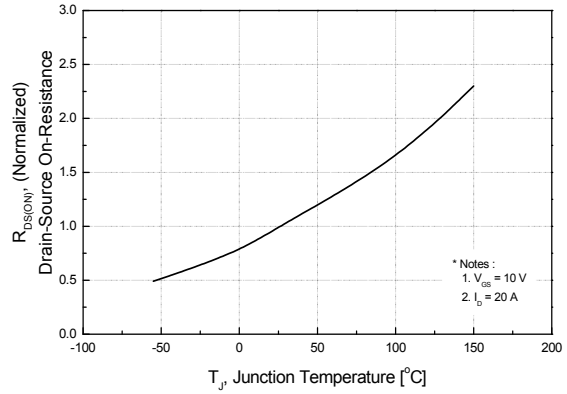


Figure 9. Maximum Safe Operating Area

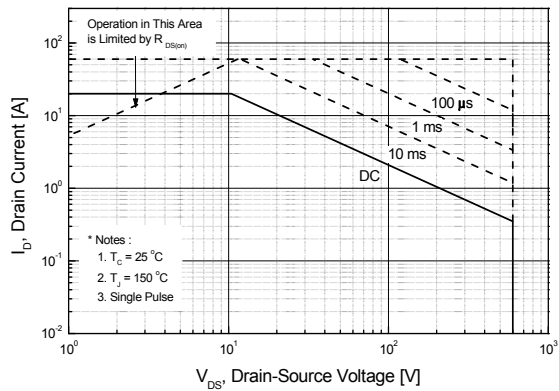


Figure 10. Maximum Drain Current vs. Case Temperature

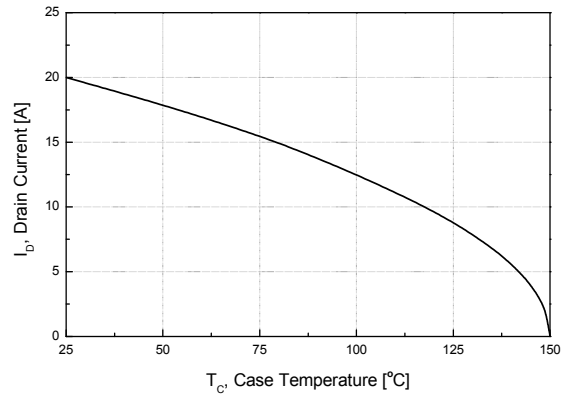
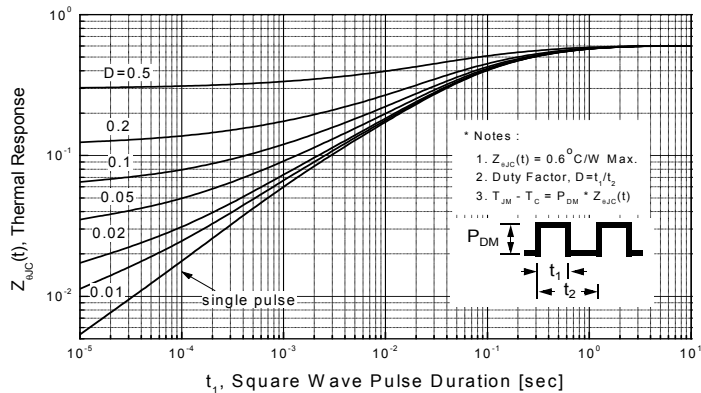


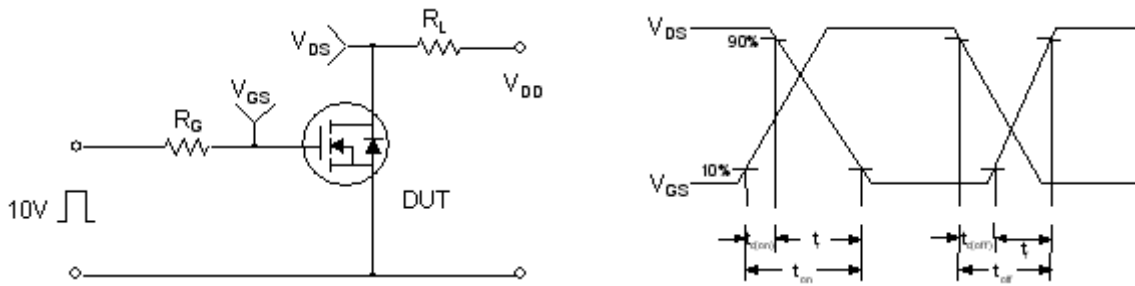
Figure 11. Transient Thermal Response Curve



Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

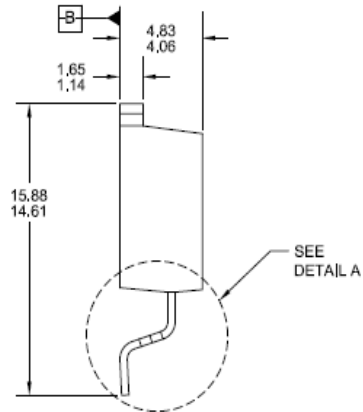
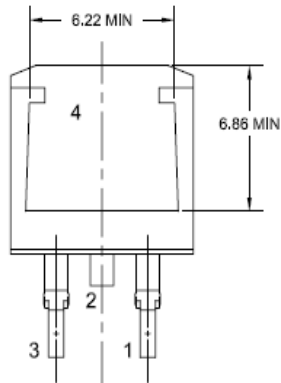
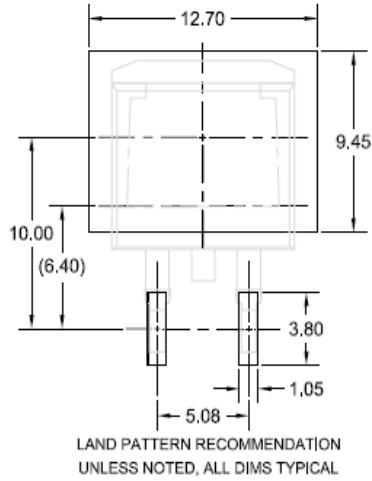
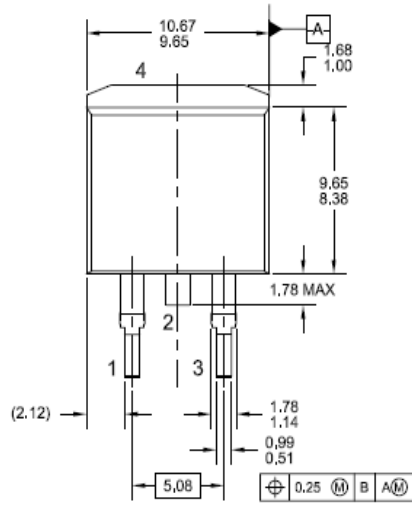


Peak Diode Recovery dv/dt Test Circuit & Waveforms

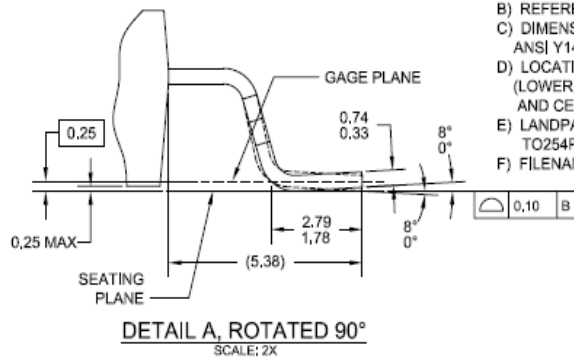


Mechanical Dimensions

D²PAK



- NOTES: UNLESS OTHERWISE SPECIFIED
 A) ALL DIMENSIONS ARE IN MILLIMETERS.
 B) REFERENCE JEDEC, TO-263, VARIATION AB.
 C) DIMENSIONING AND TOLERANCING PER ANSI Y14.5M - 1994.
 D) LOCATION OF THE PIN HOLE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE).
 E) LANDPATTERN RECOMMENDATION PER IPC TO254P1524X482-3N
 F) FILENAME: TO263A02REV6





Dimensions in Millimeters



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